

MAP 2006 PROGRAM

MONDAY 30 October

13:00 ~ 13:10 **Opening Remark** ARGOS (1F)

13:10 ~ 14:45 **SESSION 1: Invited Talks**

Chair: Eisaku Ohtsuru (Kyushu University)

13:10~13:45 1.1 **MEMS Packaging**

Masayoshi Esashi

Tohoku University (Japan)

13:45~14:15 1.2 **Silicon Valley Venture History**

Joseph Fjelstad

Silicon Pipe Inc. (U.S.A.)

14:15~14:45 1.3 **Rapid Growth of Design Houses in North China and its Chances for Japan**

Esther Liu, Arthur Wu

Semiconductor Manufacturing International (Beijing) Corp. (China)

14:45 ~ 15:00 **COFFEE BREAK**

15:00 ~ 16:00 **SESSION 2 : System in a Package and Device Embedded Technology**

Chair: Yangdo Kim (Pusan National University)

15:00~15:20 2.1 **Embedding Discrete Components inside PCB Structure**

Risto Tuominen

Imbera Electronics Oy (Finland)

15:20~15:40 2.2 **Advanced Soldering Paste Suitable for Package Stacking Process**

Tadashi Maeda

Panasonic Factory Solutions Co., Ltd. (Japan)

15:40~16:00 2.3 **SiP Development; Chip-Stacked Package in the Future**

Mamoru Kajihara

NEC Electronics Corp. (Japan)

16:00 ~ 16:20 **COFFEE BREAK**

16:20 ~ 17:40 SESSION 3 : Wafer Level Processing

Chair: Joseph Fjelstad (SiliconPipe Inc.)

- 16:20~16:40 3.1 **Eliminating Re-test Caused by Poor Probing Contact and Enabling One Million Contact's Test Probe Life on BGA/LGA Package Tests with an Effective Combination of Twist-Probe and On-line Restore**
Shigeo Kobayashi*, Michihide Ishida**
**SELASTER Corporation, **TECHNO-SEM Laboratory Co., Ltd. (Japan)*
- 16:40~17:00 3.2 **Plasma Etching Technology for Wafer Thinning Process – Plasma Stress Relief Process and Plasma Dicing Process**
Kiyoshi Arita
Panasonic Factory Solutions Co., Ltd. (Japan)
- 17:00~17:20 3.3 **Cooper Plating Techniques for Through Wafer Vias**
Sergey Savastiouk, Chih-Yang Li
ALLVIA, Inc. (U.S.A)
- 17:20~17:40 3.4 **Cu Via Filling and Interconnection Process for 3D Stack Package**
Kwang-Yong Lee, Teck-Su Oh, Jae-Ho Lee, Tae-Sung Oh
Hongik University (Korea)

18:00 ~ 20:00 RECEPTION PARTY (TINGA TINGA 5F)
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TUESDAY 31 October

09:00 ~10:20 SESSION 4: Advanced Materials and Package

Chair: Seiichiro Yoshida (New Japan Radio Co., Ltd.)

- 09:00~09:20 4.1 **Fabrication of W-Cu Composite for the Heat-sink Materials**
Young Jung Lee*, Hai-gon Kim*, Dae-Gun Kim*, Deok-Soo Kim*,
Young Do Kim*
**Hanyang University(Korea)*
***National Institute of Advanced Industrial Science and Technology(Japan)*
- 09:20~09:40 4.2 **The Inter-Connected Behavior of Au/Pd/Ni-P Plating**
Ken Sugiura, Kenji Takakura
Fukuryo Semiconductor Engineering Corp. (Japan)
- 09:40~10:00 4.3 **LTCC Multi-layer Substrate Utilized with Ink-jet and Thin Film Fine Patterning Technology**
Koji Koiwai
KOA Corporation (Japan)

10:00~10:20 4.4 **SnAgCu Optimization for Drop Reliability on Electrolytic Ni-Au Plating CSP**
Tokuro Yamaki
Senju Metal Industry Co., Ltd. (Japan)

10:20 ~ 10:40 COFFEE BREAK

10:40 ~ 12:00 **SESSION 5: MEMS and Fine Interconnection**

Chair: Jae-Ho Lee (Hongik University)

10:40~11:00 5.1 **Growing Silicon Based MEMS – The Role of Silicon Wafers and Materials Supplier**

M.Till

Okmetic Oyj (Finland)

11:00~11:20 5.2 **Wafer Level Packaged RF MEMS SPDT Switch with Thermal Driven Bimorph Cantilever**

Kiyoto Nakamura*, Hirokazu Sanpei*, Yoshiaki Moro*, Takashi Watanabe*, Masayoshi Esashi**

**ADVANTEST Laboratories Co., Ltd.(Japan), ** Tohoku University(Japan)*

11:20~11:40 5.3 **Laser Assisted Interconnection Technology for MEMS and Wafer Level Packaging**

Elke Zakel

PacTech-Packaging Technologies GmbH (Germany)

11:40~12:00 5.4 **Roll to Roll Screen Printer System for Fine Pitch Patterning on PET Film Roll or TAB Tape Materials**

Hajime Fukawa

Produce Corp. (Japan)

12:00 ~ 14:00 LUNCH BREAK

14:00 ~ 15:00 **SESSION 6: Design and Analysis**

Chair: Donghwan Kim (Korea University)

14:00~14:20 6.1 **Strain Measurement in Electronic Packages using the Digital Image Correlation Method**

Toru Ikeda, Nobuyuki Shishido, Noriyuki Miyazaki

Kyoto University (Japan)

- 14:20~14:40 6.2 **FSM Metrology Tools for BEOL**
 Uwe Wielsch*, Ann Koo*, Haruo Akimoto**
 *Frontier Semiconductor (U.S.A.)
 **Frontier Semiconductor Japan Branch Office (Japan)
- 14:40~15:00 6.3 **High Power Linear Amplifier for WiMAX**
 Kazuyoshi Kikuta
 D-CLUE Technologies Co., Ltd. (Japan)

15:00 ~ 15:20	COFFEE BREAK
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15:20 ~ 17:00 **SESSION 7: Test and Technology Road Map**

Chair: Daisuke Yamaguchi (ATE Service Corp.)

- 15:20~15:40 7.1 **Testing Industry Benchmark –King Yuan Electronics Co., Ltd. (KYEC)**
 Toshio Sugano
King Yuan Electronics Co., Ltd. (Taiwan)
- 15:40~16:00 7.2 **Design for Business: Advancing the Business Culture of Semiconductor Back-End Manufacturing**
 Andres Carrasco, Masayuki Kayama
Nagase Electronic Equipment Service Co., Ltd. (Japan)
- 16:00~16:20 7.3 **Introduction of World Major Technology Roadmap for Electronics and Gap Analysis between Jisso Technology Roadmap 2005**
 Henry H.Utsunomiya
Interconnection Technologies, Inc. (Japan)
- 16:20~16:40 7.4 **Investment Opportunities in the Electronics Industry in Malaysia**
 Zabidi Mahbar
Malaysian Industrial Development Authority(Malaysia)
- 16:40~17:00 7.5 **Making Arrangements**
 Ryan Xu
Beijing Tsinghua Tongfang Microslevtronics Co., Ltd.(China)

17:00 ~ 19:00 **SESSION 8: Poster Presentation with wines** NAVIS(1F)

Chair: Shigemitsu Tashiro (JETRO Fukuoka)